IDEC Chip Design Contest

An ADC-based Asynchronous Eye Monitor for 56Gb/s PAM-4 Links

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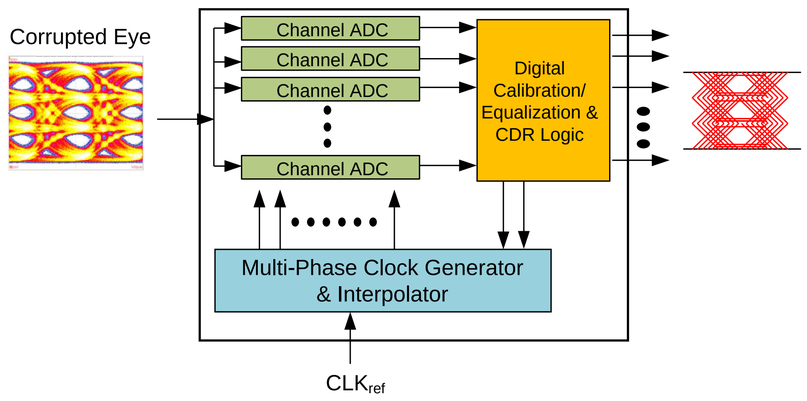
Abstract

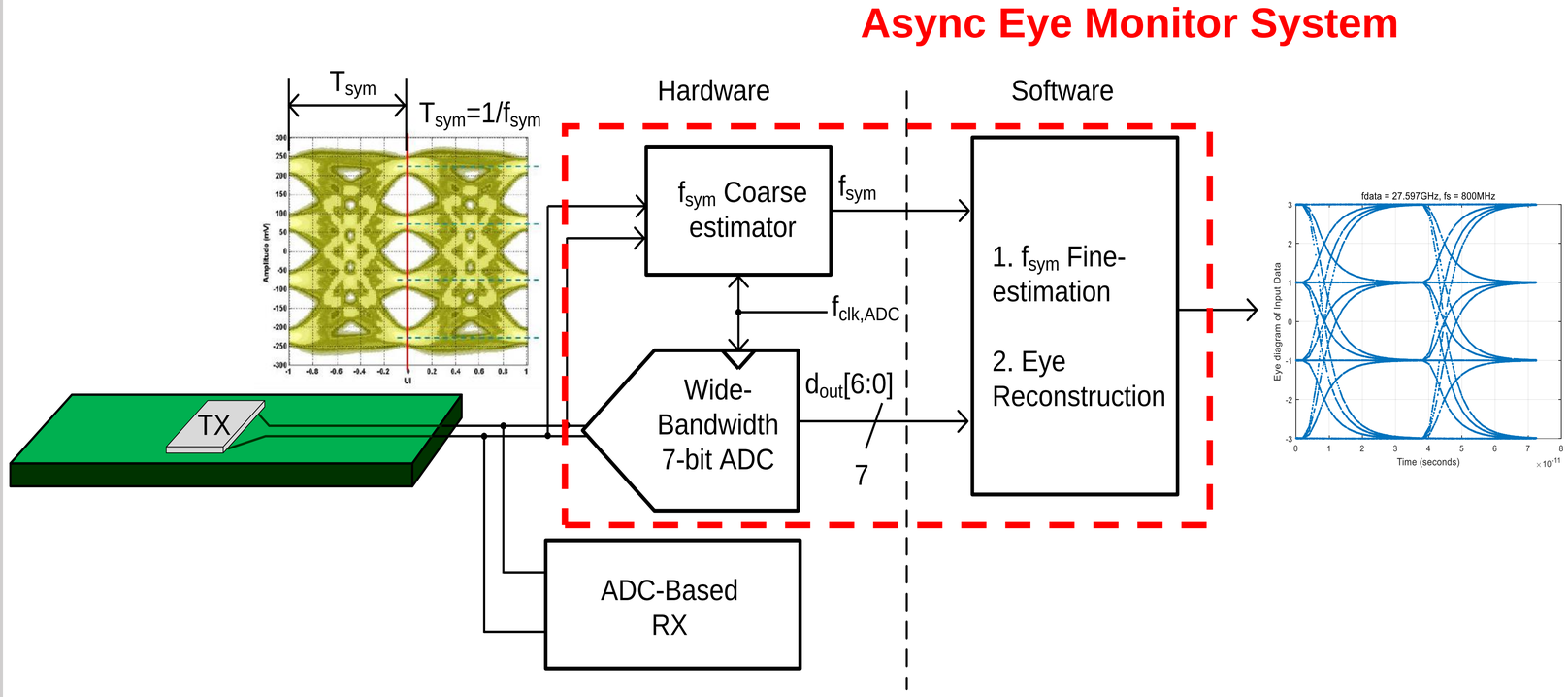
High-Speed Serial-Link Receiver



- These days, there is a growing demand for high data rates in high-speed serial links.
- Eye monitor is often used to guarantee the quality of signal patterns for reliable link performance.
- Data Converters are essential building blocks in memory and high-speed I/O interface.
- NRZ encoding is increasingly replaced by PAM-4

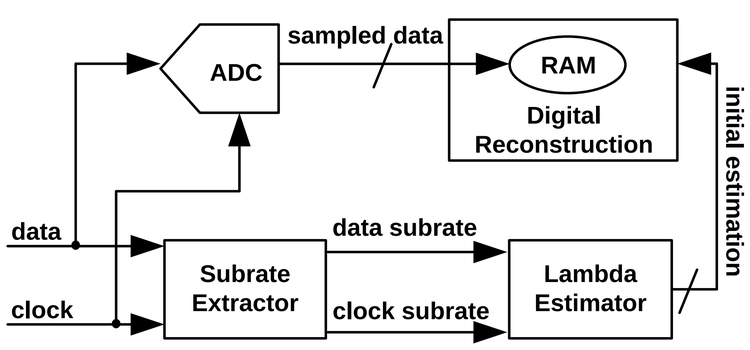
→ **We present an asynchronous eye monitor based on a wideband 7-bit SAR ADC for observing the signal integrity in high-speed serial links.**
(Especially PAM-4 links)

High-speed I/O systems and An ADC-based Asynchronous Eye Monitor

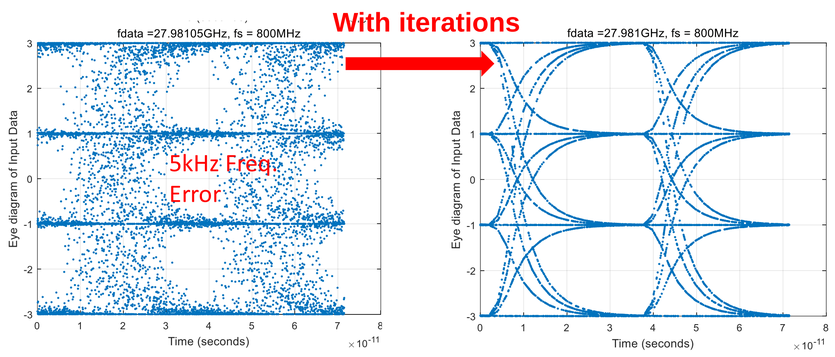


- We use a wide-bandwidth sampling of slice ADC to sub-sample the incoming PAM-4 data steam
- We can estimate the symbol clock frequency from PRBS data, and reconstruct the eye diagram in software
- It is verified by a behavioral simulation model of PAM-4 transceiver with realistic channel model

Architecture of an ADC-based Asynchronous Eye Monitor and Simulation Results



(a) Block Diagrams of an Eye Monitor

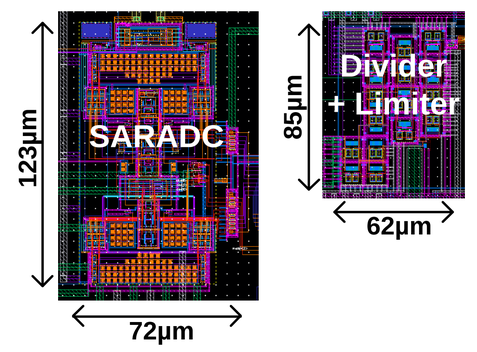


(b) Reconstructed Eye Diagram

- Figure (a) is the block diagram of an eye monitor.
- The algorithm, implemented in software, has been tested for symbol rate ranging form 10Gbps to 60Gbps, showing highly linear correlation between digital output from coarse estimator and actual PRBS symbol rate.
- Then, we can get an optimal symbol frequency by estimating course frequency and implementing lots of iterations.
- Finally, we can reconstruct the eye diagram with the fine tune process.
- Key building blocks in the eye monitor system include a 7-bit SAR ADC and a high-speed CML divider, both of fabricated in 65nm CMOS process.

Conclusion

Die Photo (ADC + Divider + Limiter)



- Digital Synthesis structure is fabricated by FPGA.

	Traditional Asynchronous Eye Monitor[1]	Proposed Asynchronous Eye Monitor
Signal Encoding	NRZ encoding	PAM-4
ADC Sampling Frequency	200MHz	800MHz
Process	65nm CMOS	65nm CMOS
Target Signal Frequency	10Gbps	56Gbps

[1] Zheng, Shijie, M. Eng. Massachusetts Institute of Technology, "A low cost asynchronous eye diagram reconstruction system for high speed links," Massachusetts Institute of Technology. Department of Electrical Engineering and Computer Science, pp. 1-98, 2013.